CLAIMS

What is claimed is:

1. A chip-scale package comprising:

a semiconductor die having an active surface having at least one bond pad thereon;

at least one conductive trace having an upper surface and a lower surface, the lower surface of said conductive trace substantially non-conductively attached to a portion of the active surface of said semiconductor die;

at least one conductive bond connecting the at least one conductive trace to the at least one bond pad on the active surface of said semiconductor die;

at least one carrier bond attached to the upper surface of the at least one conductive trace; and

an encapsulant material encapsulating said semiconductor die, the at least one conductive trace, the at least one conductive bond and a portion of the at least one carrier bond, the at least one carrier bond having another portion extending beyond said encapsulant material.

2. A chip-scale package comprising:

a semiconductor die having an active surface having a plurality of bond pads thereon;

a dielectric element having an upper surface and a lower surface, the lower surface of said laminate attached to a portion of the active surface of said semiconductor die;

a plurality of conductive traces, each trace of the plurality of conductive traces having an upper surface and a lower surface, the lower surface of each trace of said plurality of conductive traces attached to a portion of the upper surface of said dielectric element for connecting each conductive trace of said plurality of conductive traces to the active surface of said semiconductor die;

a plurality of conductive bond members, at least one conductive bond member of the plurality of conductive bond member connecting each conductive trace of said plurality of conductive traces to at least one bond pad of the plurality of bond pads on the active surface of said semiconductor die;

a plurality of conductive carrier bonds, at least one carrier bond disposed on the upper surface of each conductive trace of said plurality of conductive traces; and

an encapsulating material disposed about at least portions of said semiconductor die, said dielectric element, said plurality of conductive traces, said plurality of bond wires and a portion of each carrier bond of said plurality of carrier bonds.

3. A chip-scale package as in claim 2, wherein said dielectric element includes an adhesive-coated polyimide tape.

4. A chip-scale package as in claim 2, wherein said dielectric element includes a polyimide film.

5. A chip-scale package as in claim 2, wherein the upper surface and lower surface of said dielectric element are attached respectively to a portion of the lower surface of each conductive trace of said plurality of conductive traces and a portion of the active surface of said semiconductor die connecting portions of said plurality of conductive traces and portions of said semiconductor die.

6. A chip-scale package as in claim 2, wherein said plurality of conductive traces comprise a plurality of lead fingers.

7. A chip-scale package as in claim 2, wherein said plurality of conductive traces comprise a conductive metal.

8. A chip-scale package as in claim 2, wherein said plurality of conductive bond members comprise a conductive metal.

9. A chip-scale package as in claim 2, wherein said plurality of conductive bond members comprise bond wires.

10. A chip-scale package as in claim 9, wherein said bond wires comprise gold or aluminum.

11. A chip-scale package as in claim 2, wherein said plurality of conductive bond members comprise TAB bonds.

12. A chip-scale package as in claim 2, wherein said plurality of conductive bond members comprise thermocompression bonds.

13. A chip-scale package as in claim 2, wherein said plurality of carrier bonds include metal.

14. A chip-scale package as in claim 2, wherein said plurality of carrier bonds comprise a conductive or conductor-filled polymer.

15. A chip-scale package as in claim 2, wherein said plurality of carrier bonds are selectively located on the upper surface of said plurality of conductive traces forming an array.

16. A chip-scale package as in claim 2, wherein said plurality of carrier bonds comprise solder balls.

17. A chip-scale package as in claim 2, wherein said encapsulating material comprises a substantially non-conductive material.

18. A chip-scale package as in claim 2, wherein said encapsulating material comprises a material having a low modulus of elasticity.

19. A chip-scale package as in claim 2, wherein each carrier bond of said carrier bonds further comprises an upper portion and a lower portion, said lower portion of a carrier bond attached to the upper surface of a conductive trace of said plurality of conductive traces.

20. A chip-scale package as in claim 19, wherein said encapsulating material is disposed about the lower portions of said carrier bonds.

21. A method for fabricating a chip-scale package comprising:

providing a semiconductor die having an active surface having at least one bond pad disposed thereon;

providing at least one conductive trace having an upper surface and a lower surface;

dielectrically attaching at least a portion of the lower surface of said at least one conductive trace to a portion of the active surface of said semiconductor die;

attaching a conductive bond member between said at least one conductive trace and the at least one bond pad disposed on the active surface of said semiconductor die;

attaching at least one carrier bond to a portion of the upper surface of said at least one conductive trace; and

encapsulating at least portions of said semiconductor die, said at least one conductive trace, said conductive bond and a portion of said at least one carrier bond.

22. The method for fabricating a chip-scale package as in claim 21, further comprising forming said at least one conductive trace as a lead frame element.

23. The method for fabricating a chip-scale package as in claim 21, further comprising forming said at least one conductive trace of a conductive metal.

24. The method for fabricating a chip-scale package as in claim 21, further comprising forming said conductive bond member as a wire bond.

25. The method for fabricating a chip-scale package as in claim 21, further comprising forming said conductive bond member as a TAB bond.

26. The method for fabricating a chip-scale package as in claim 21, further comprising forming said at least one carrier bond as a solder ball.

27. The method for fabricating a chip-scale package as in claim 21, further comprising forming said at least one carrier bond comprises an electrically conductive or conductor-filled polymer.

28. The method for fabricating a chip-scale package as in claim 21, wherein said dielectrically attaching is effected using a polyimide tape.

29. A method for fabricating a chip-sized package as in claim 21, wherein the step of dielectrically attaching at least a portion of the lower surface of said conductive trace to a portion of the active surface of said semiconductor die further comprises:

providing a dielectric material having an upper surface and a lower surface;

attaching at least a portion of the lower surface of said joint material to at least a portion of the active surface of said semiconductor die; and

attaching at least a portion the lower surface of said at least one conductive trace to at least a portion of the upper surface of said joint material.